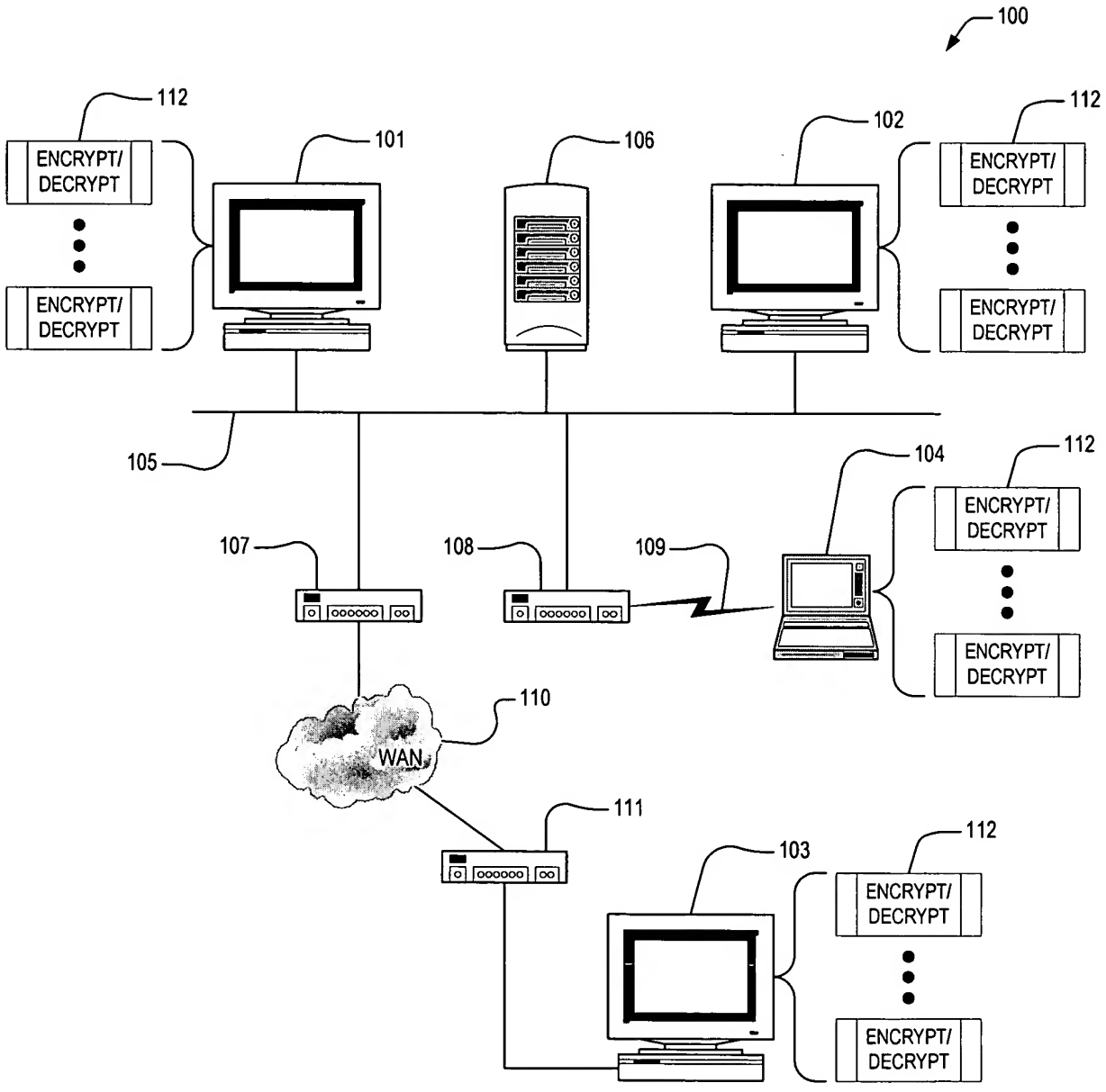
100
112
ENCRYPT/
DECRYPT
ENCRYPT/
DECRYPT
101
106
102
112
ENCRYPT/
DECRYPT
ENCRYPT/
DECRYPT
105
104
112
ENCRYPT/
DECRYPT
ENCRYPT/
DECRYPT
107
108
109
110
WAN
111
103
112
ENCRYPT/
DECRYPT
ENCRYPT/
DECRYPT

FIG. 1

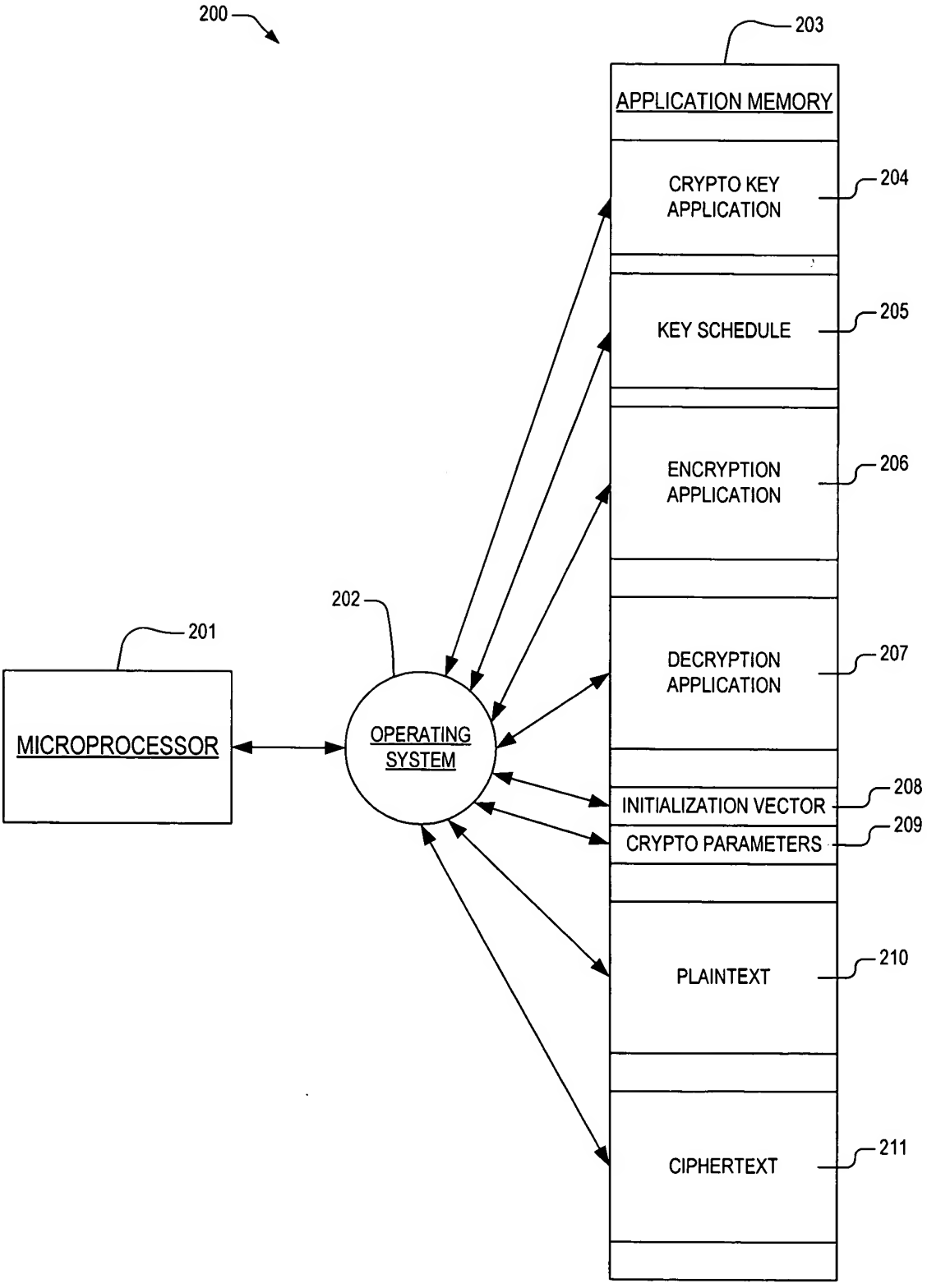
200
203
APPLICATION MEMORY
CRYPTO KEY APPLICATION
204
KEY SCHEDULE
205
ENCRYPTION APPLICATION
206
DECRYPTION APPLICATION
207
INITIALIZATION VECTOR
208
CRYPTO PARAMETERS
209
PLAINTEXT
210
CIPHERTEXT
211
202
OPERATING SYSTEM
201
MICROPROCESSOR

FIG. 2

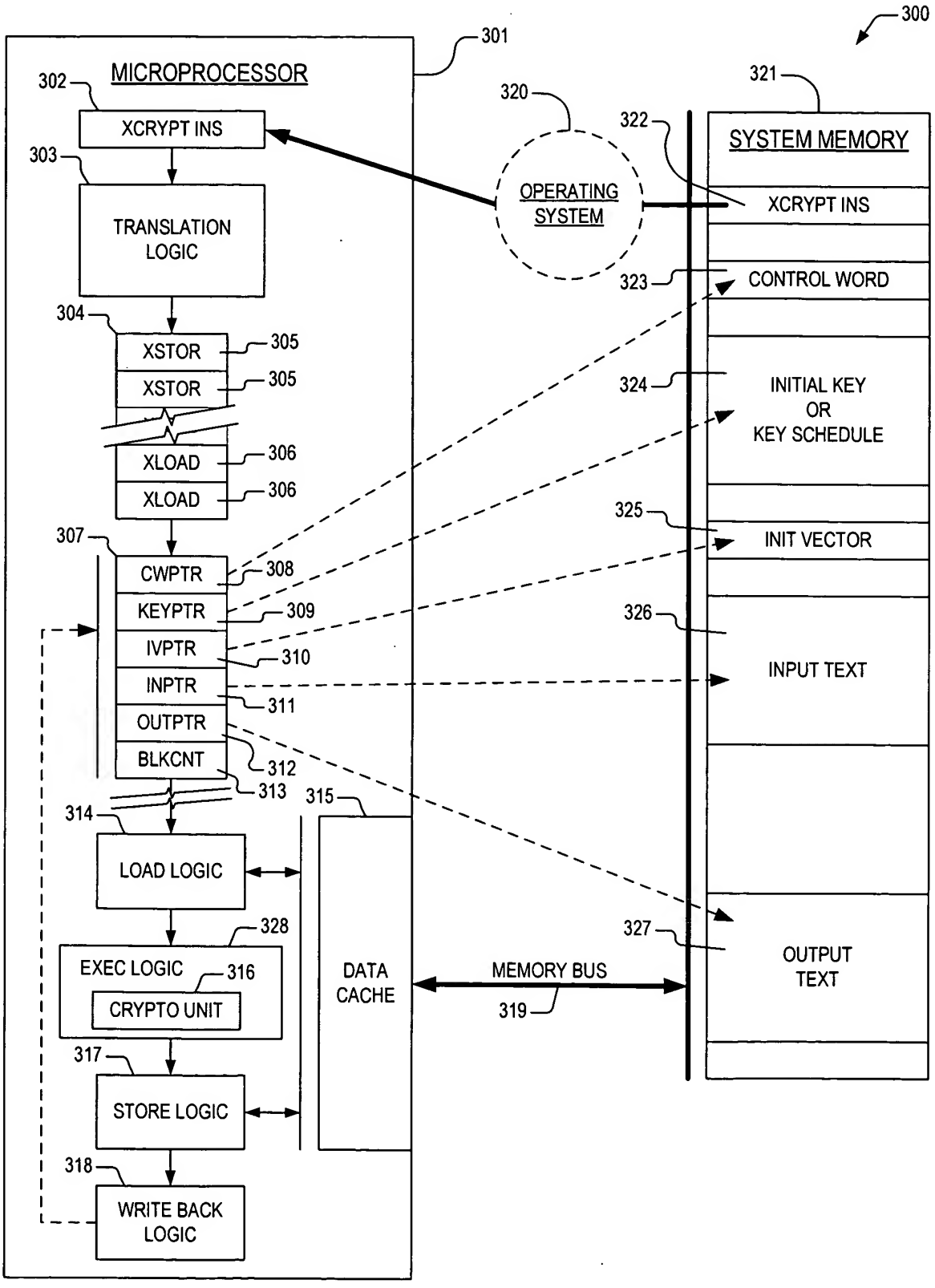
300
301
MICROPROCESSOR
302
XCRYPT INS
303
TRANSLATION LOGIC
304
XSTOR
305
XSTOR
305
XLOAD
306
XLOAD
306
307
CWPTR
308
KEYPTR
309
IVPTR
310
INPTR
311
OUTPTR
BLKCNT
312
313
314
LOAD LOGIC
315
328
EXEC LOGIC
316
CRYPTO UNIT
317
STORE LOGIC
318
WRITE BACK LOGIC
DATA CACHE
MEMORY BUS
319
320
OPERATING SYSTEM
321
SYSTEM MEMORY
322
XCRYPT INS
323
CONTROL WORD
324
INITIAL KEY OR KEY SCHEDULE
325
INIT VECTOR
326
INPUT TEXT
327
OUTPUT TEXT

FIG. 3

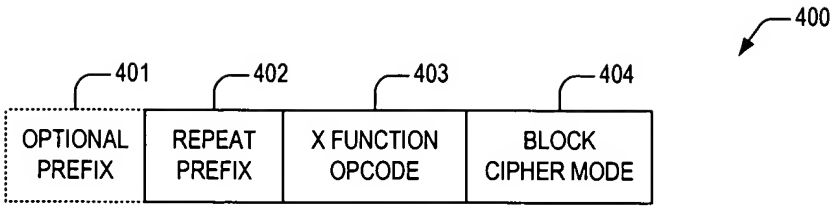

FIG. 4

500

BCM VALUE	MODE
0xC8	ELECTRONIC CODE BOOK (ECB)
0xD0	CIPHER BLOCK CHAINING (CBC)
0xE0	CIPHER FEEDBACK (CFB)
0xE8	OUTPUT FEEDBACK (OFB)
ALL OTHER VALUES	RESERVED

FIG. 5

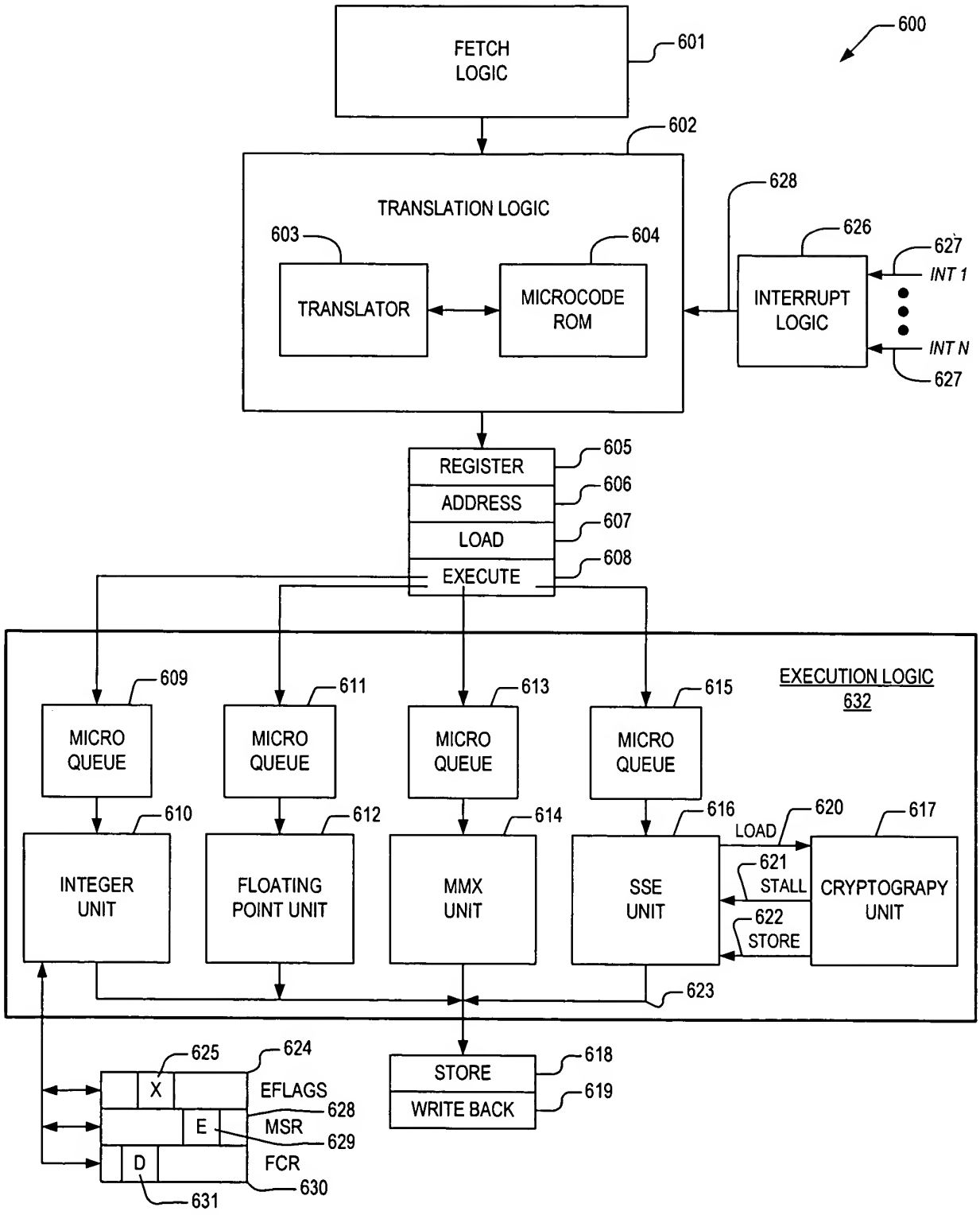
FETCH LOGIC
601
600
602
TRANSLATION LOGIC
603
TRANSLATOR
604
MICROCODE ROM
628
626
627
INTERRUPT LOGIC
INT 1
INT N
627
REGISTER
ADDRESS
LOAD
EXECUTE
605
606
607
608
609
611
613
615
EXECUTION LOGIC 632
MICRO QUEUE
MICRO QUEUE
MICRO QUEUE
MICRO QUEUE
610
612
614
616
620
617
INTEGER UNIT
FLOATING POINT UNIT
MMX UNIT
SSE UNIT
LOAD
621
STALL
622
STORE
CRYPTOGRAPY UNIT
623
625
624
X
EFLAGS
E
MSR
628
629
D
FCR
630
631
STORE
WRITE BACK
618
619

FIG. 6

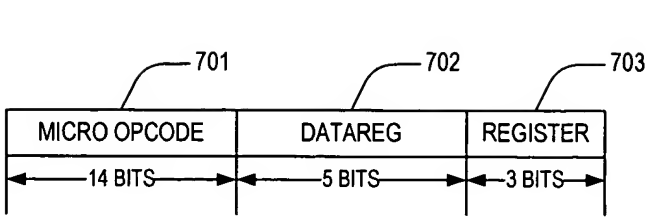

FIG. 7

800

VALUE	OPERATION
000	RESERVED
001	RESERVED
010	LOAD CONTROL WORD (CW) REGISTER
011	RESERVED
100	LOAD INPUT-0 (IN-0) REGISTER AND START CRYPTOGRAPHY UNIT
101	LOAD INPUT-1 (IN-1) REGISTER
110	LOAD CRYPTO KEY-0 REGISTER (LOWER 128 BITS OF KEY)
111	LOAD CRYPTO KEY-1 REGISTER (UPPER 128 BITS OF KEY)

FIG. 8

900

VALUE	OPERATION
000	RESERVED
001	RESERVED
010	RESERVED
011	RESERVED
100	STORE OUTPUT-0 (OUT-0) REGISTER
101	STORE OUTPUT-1 (OUT-1) REGISTER
110	RESERVED
111	RESERVED

FIG. 9

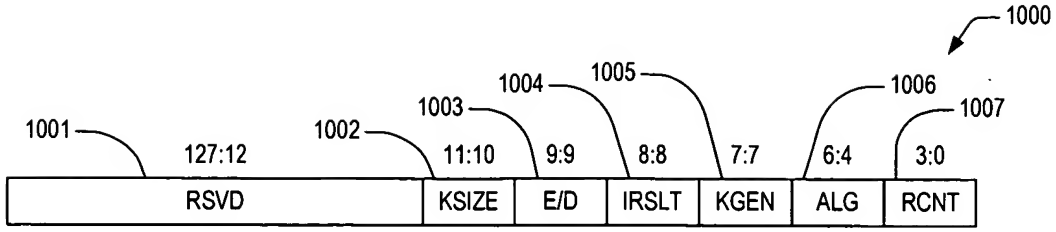
1000
1001
127:12
RSVD
1002
1003
11:10
KSIZE
1004
9:9
E/D
1005
8:8
IRSLT
7:7
KGEN
1006
6:4
ALG
1007
3:0
RCNT

FIG. 10

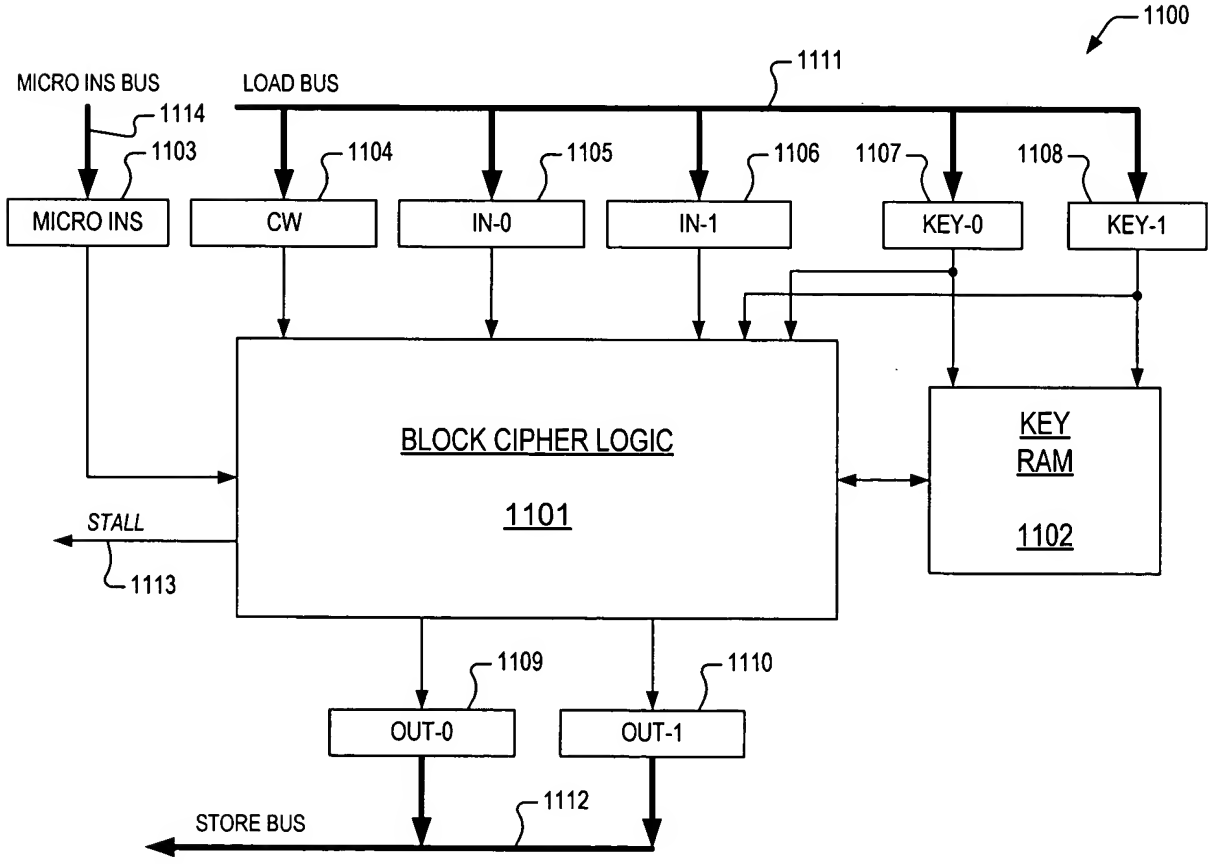
1100
MICRO INS BUS
LOAD BUS
1111
1114
1103
1104
1105
1106
1107
1108
MICRO INS
CW
IN-0
IN-1
KEY-0
KEY-1
BLOCK CIPHER LOGIC
1101
KEY
RAM
1102
STALL
1113
1109
1110
OUT-0
OUT-1
1112
STORE BUS

FIG. 11

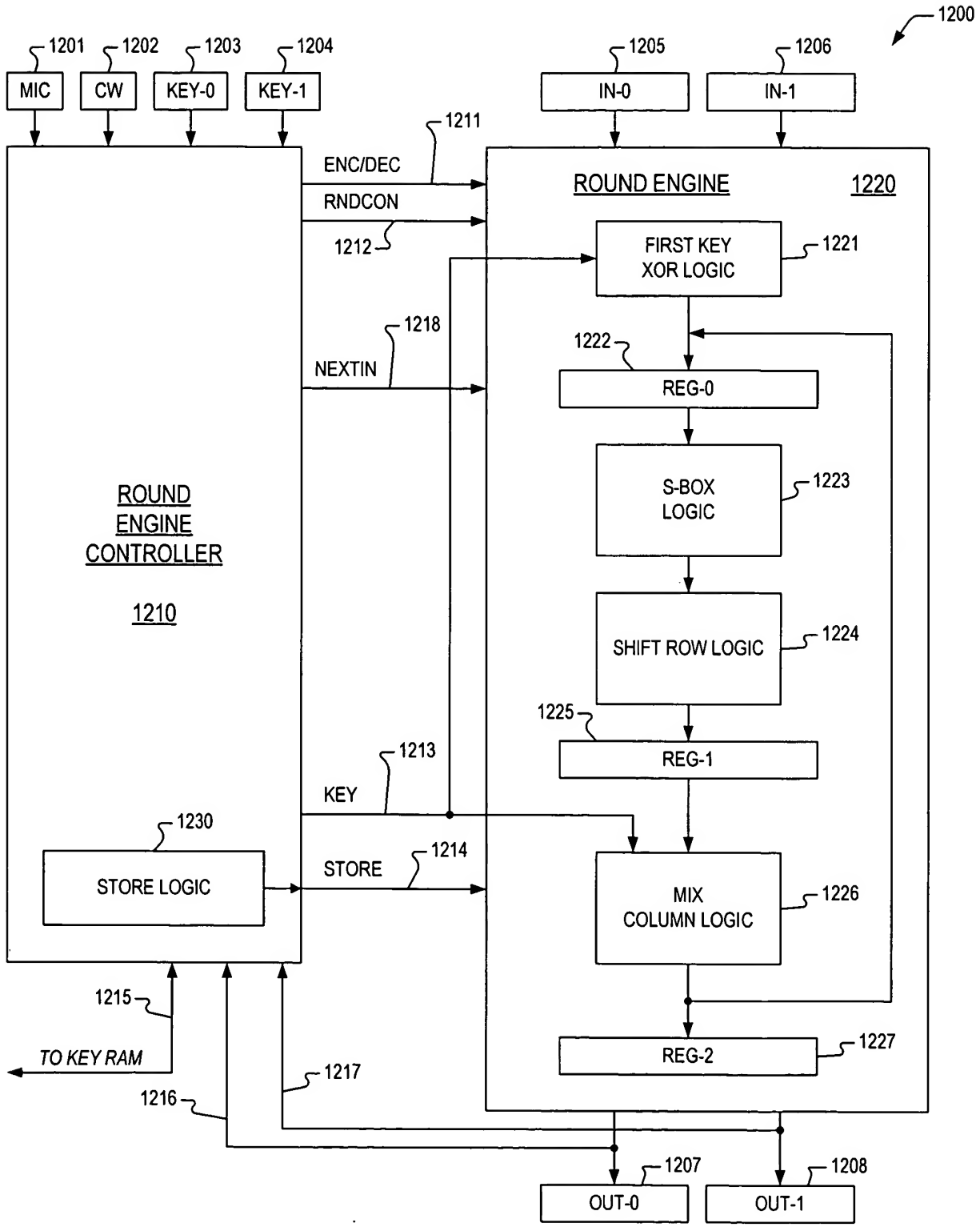
1200
1201
MIC
1202
CW
1203
KEY-0
1204
KEY-1
1205
IN-0
1206
IN-1
1211
ENC/DEC
RNDCON
1212
ROUND ENGINE
1220
FIRST KEY XOR LOGIC
1221
1218
NEXTIN
1222
REG-0
S-BOX LOGIC
1223
ROUND ENGINE CONTROLLER
1210
SHIFT ROW LOGIC
1224
1225
REG-1
1213
KEY
1230
STORE LOGIC
STORE
1214
MIX COLUMN LOGIC
1226
1215
TO KEY RAM
REG-2
1227
1217
1216
1207
OUT-0
1208
OUT-1

FIG. 12

1300

MICRO INSTRUCTION	COMP CYCLE
LD.IN-0	2
ST.OUT-0	24
LD.IN-0	26
ST.OUT-0	48
LD.IN-0	50
ST.OUT-0	72

24 CYCLES/BLOCK

24 CYCLES/BLOCK

FIG. 13

1400

MICRO INSTRUCTION	COMP CYCLE
LD.IN-0	2
LD.IN-0	4
ST.OUT-0	24
LD.IN-0	26
ST.OUT-0	44
LD.IN-0	46

20 CYCLES/BLOCK

FIG. 14

1500

MICRO INSTRUCTION	COMP CYCLE	
LD.IN-1	2	
LD.IN-0	4	
ST.OUT-1	26	
ST.OUT-0	28	
LD.IN-1	30	
LD.IN-0	32	28 CYCLES/2 BLOCKS
ST.OUT-1	54	
ST.OUT-0	56	
LD.IN-1	58	
LD.IN-0	60	28 CYCLES/2 BLOCKS
ST.OUT-1	82	
ST.OUT-0	84	

FIG. 15

1600

MICRO INSTRUCTION	COMP CYCLE	
LD.IN-1	2	
LD.IN-0	4	
LD.IN-1	6	
LD.IN-0	8	
ST.OUT-1	26	
ST.OUT-0	28	
LD.IN-1	30	
LD.IN-0	32	20 CYCLES/2 BLOCKS
ST.OUT-1	46	
ST.OUT-0	48	
LD.IN-1	50	
LD.IN-0	52	

FIG. 16